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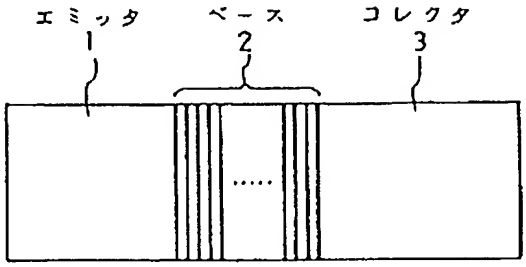
TITLE : BIPOLAR TRANSISTOR



ABSTRACT : PURPOSE: To accelerate an NPN type transistor whose base resistance is several times smaller compared with conventional ones subject to the same base layer thickness and P-type impurity concentration of the base by providing the transistor with a strain superlattice structured base layer.

CONSTITUTION: A strain superlattice is led in a base layer 2. For example, $In_{0.52}Al_{0.48}As$ is used for an emitter 1 and a collector 3 as semiconductor material while $In_{0.53+x}Ga_{0.47-x}As$ and $In_{0.53-x}Ga_{0.47+x}As$ (x=0.15) are used for a base 2 and respective elements 1, 2 and 3 are alternately laminated in thickness of 200˜ to dope P type impurity such as berillium etc. Here, the compressive force is given to an $In_{0.35+x}Ga_{0.47-x}As$ layer to increase the hole mobility assuming x=0.15 instead of x=0 up to four times at the room temperature and ten times at 77K. Thus, subject to the same base layer thickness and the P type impurity concentration, the base resistance can be reduced down to 1/2 at the room temperature and 1/5 at 77K compared with the conventional base resistance enabling high speed transistors to be manufactured.